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Multi-layer coated conductor cylinders—an alternative approach to superconducting coil fabrication

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Abstract

A radically new approach to the fabrication of electrical machines based on an HTS coated conductor has been developed. Instead of long lengths of coated conductor tape being wound into coils in a conventional manner, we propose to use a combination of thin film deposition and patterning techniques with an essentially coaxial cylindrical geometry to produce superconducting multilayer coils. These patterned coated conductor cylinders can subsequently be configured in different ways to form a variety of superconducting electrical machines all based on highly manufacturable 'standard' cylindrical modules with high engineering current density. The cost benefits of such standardized manufacturing may be very significant in future applications of coated conductor. Multi-layer thin films of YBCO on buffered, curved Ni-based, textured substrates have been grown by pulsed laser deposition in order to demonstrate the feasibility of fabricating, *in situ*, a multi-turn coil on a cylindrical former by continuous deposition of sequential layers of superconductor and insulator.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

The development of scalable manufacturing processes for long lengths of high temperature superconductor (HTS) coated conductor is proceeding worldwide but progress is rather slow, despite considerable effort and funding. Using several different tape fabrication approaches, usually based on rolling assisted biaxial textured substrates, RABiTS [1, 2], ion beam assisted deposition, IBAD [3–5], or inclined substrate deposition, ISD [6], followed by buffer and ReBCO layers, the end-to-end supercurrents of tapes in lengths of the order of metres is already adequate for many applications. However, sufficient lengths of high performance tapes are not available for anything other than very simple demonstrators [7].

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The essential feature of all coated conductor technologies is the copying of the biaxial texture from the substrate or buffer layer through to a single functional YBCO layer. All the current international effort on coated conductors is based on the idea of improving the technology to allow long (km) lengths of coated conductors on flexible substrates to be produced with reproducible homogeneous properties. For those applications involving coils, the tape would then be wound in the required geometry. The novel integrated design concept proposed here employs the simple expedient of producing a coil *in situ* by a multi-layer deposition sequence onto a rotating cylindrical former.

Systems designers are likely to have to wait many years before sufficient conductor is produced to wind 'real' coils and to be able to demonstrate electrical machines before

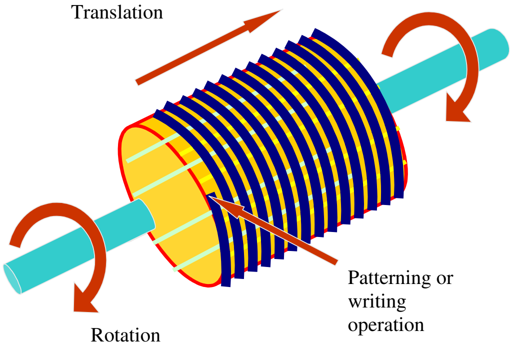

Figure 1. Buffer and YBCO layer deposition on an IBAD textured former followed by laser scribing to 'pattern' a coil—similar to a screw cutting operation on a lathe. A similar structure could be achieved by an IBAD beam writing process followed by buffer and YBCO layer depositions.

proceeding to full scale manufacture on a commercial basis. However, as a result of these scale-up attempts, and the increased understanding of the key materials issues during the past five years, many of the film deposition processes and multilayer architectures are actually well positioned to adopt an alternative approach based on a coaxial, essentially cylindrical geometry, an example of which is shown schematically in figure 1. In this approach, layers may be uniformly deposited and subsequently patterned to define the conducting tracks, to mimic a helical winding, or in some cases direct beam writing or masking processes may be employed to define the coil [8].

The principle of the novel approach is that, if the biaxial texture can be transmitted through the buffer layer architecture into an initial YBCO layer, it should also be possible to continue copying this texture through subsequent layers to produce a multi-layer structure of electrically isolated superconducting elements which, on a cylindrical former, could provide the basis of a multi-turn, multi-layered, helical superconducting coil. To fabricate a superconducting coil *in situ* a single cylindrical textured base substrate mounted on a cylindrical heater provides the template for the whole process. The base substrate could be a helically wound textured RABiTS Ni tape, an *ex situ* prepared IBAD tape of textured YSZ on Ni or Hastelloy, a textured IBAD YSZ coating on a cylindrical base substrate, or an ISD textured layer. The buffer layers and/or superconducting layer are then deposited onto the base substrate, using an appropriate processing route, while rotating and translating the heater. A suitably lattice-matched insulating layer is subsequently deposited followed by another YBCO layer with textured overlayer shunt. This combination is then repeated to provide a multi-layer YBCO coil with each layer electrically isolated, and if necessary, each layer protected by a metallic shunt layer. Only one layer of base substrate is required to provide the initial texture, thus dramatically reducing cost and, even more, significantly increasing J_e (the 'engineering current density'), since by far the largest (in terms of cross-sectional area) component of the conventional single-YBCO-layer coated conductor tape is the base substrate. This greatly increased J_e means that the strict requirement on texture-copying through the layers can be relaxed to some extent. However, if degradation of epitaxy is observed as the number of layers is increased, it may be necessary to add a new template layer at intervals.

This paper reports the details of this novel design concept and the advantages it has when compared to the conventional approach based on windings. Preliminary, proof-of-principle experiments to establish the feasibility of the growth of textured multi-layers on a Ni tape supported on a cylindrical heater are reported.

2. Comparisons between processing of long lengths and cylinders

There are many lessons to be learnt from attempts worldwide to process long lengths of coated conductors over the last few years, and indeed this is what has partly prompted us to re-examine the goals of mainstream coated conductor research and the obstacles to achieving these goals. When one considers that many of the applications require multilayer windings, and that many of the potential end-uses are in solenoid magnets or rotating machinery (e.g. motors, generators etc), the idea of processing in the form of cylindrical artifacts mounted on rotating shafts presents itself. Once this 'integrated manufacturing' process with coaxial geometry is grasped, a number of simplifications follow for both process developer and systems designer alike.

HTS film deposition techniques which are currently under development for the manufacturing of long lengths of coated conductor include thermal evaporation [9], sputter deposition [10], pulsed laser deposition (PLD) [1, 2], liquid phase epitaxy (LPE) [11], various chemical vapour deposition processes (MOCVD) [12], spray pyrolysis [13] and deposition processes whereby precursors are applied, often in sol–gel form, and subsequently heat-treated [14]. Each of these potential large-scale manufacturing techniques has its own merits and demerits in terms of layer quality, process complexity, process stability (for high uniformity), number of process steps, speed and cost. It is not appropriate here to go into great detail, but there are some fundamental points which should be made when comparing the potential techniques for scale-up whether one is considering processing of long tape lengths or processing in the coaxial geometry.

The first fundamental point we would make is that layer quality must ultimately be judged by the ability of the ReBCO layer to carry end-to-end current. High currents will only be attainable if

(i) layer quality is high for reasonable film thicknesses (i.e. the product of J_c and film thickness is high) and
(ii) the uniformity of the conductor along its length is such that there are no weak areas in series with other areas.

This last point implies good process stability in combination with a tolerant processing window, because any variations with time will otherwise give rise to non-uniformities and a reduced I_c.

The second fundamental point is more to do with the overall layer architecture, inclusive of buffer layers and metallic stabilization layer. Complexity in buffer layer architecture should be avoided if at all possible, because every additional layer has a cost and also every interface brings its own problems of thermal expansion mismatch, diffusion profiles etc. Reduced processing temperatures are nearly always to be preferred, consistent with good layer quality

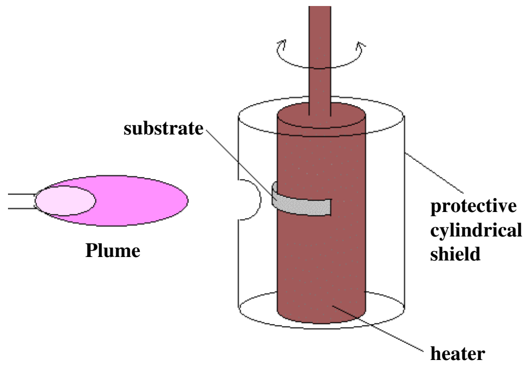

Figure 2. Schematic diagram of the rotating cylindrical heater in the PLD chamber.

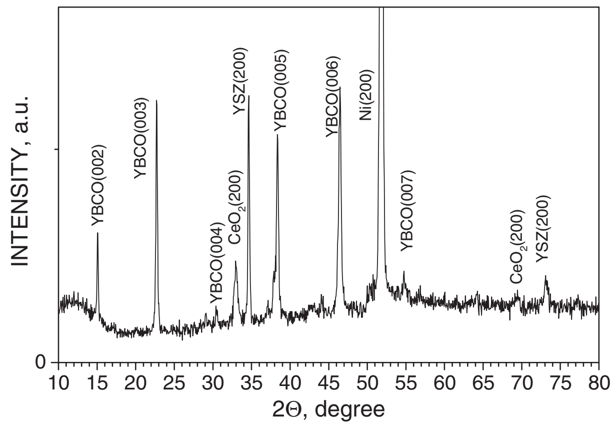

Figure 3. XRD scan of single YBCO layer on C/Y/C buffers deposited statically on a curved Ni tape.

at realistic growth rates, and it is interesting to note that the large area thermal coevaporation route is very good in this respect—and it has just one buffer layer [9]. When considering a true multilayer technology i.e. many superconducting layers separated by buffer layers and metallizations, lower processing temperatures become even more desirable to prevent unwanted diffusions and propagation of defects.

So far, most of these materials-related comments are equally applicable to both the conventional long length tape approach and the alternative cylindrical processing approach we are advocating here. However, there are two very important processing simplifications as we move towards the cylindrical processing scenario with no moving tape. The first is that although the materials requirements are quite similar, the process control aspects change dramatically. For example, a major problem with most tape scale-up routes is the difficulty in holding the substrate temperature constant (a) throughout the deposition area and (b) throughout the deposition processes. To achieve uniformity of temperature, both in time and space, the ideal scenario is to have a heated substrate with substantial thermal mass, or close thermal contact between substrate and heater. Spatial and temporal fluctuations are thus minimized. In practice, however, radiative heating is often used to heat moving tapes and problems arise due to spatial profiles in thermal conduction and, of course, changes in emissivity of surfaces as films are deposited.

In the case of film deposition on cylindrical substrates, there is no moving tape and no particular necessity for radiative heating. In fact, the cylindrical substrate can incorporate an integral heater, with the coaxial symmetry resulting in a high degree of temperature uniformity and the thermal mass of the substrate (or support thereof) being such as to minimize the effect of any local temperature fluctuations during processing. The integral heater can incorporate sensors for temperature control with different zones if necessary (as is standard practice for tube furnaces) to ensure a uniform temperature over the cylinder's surface.

The second important process simplification is another direct result of the coaxial symmetry and the simple ability to rotate the cylinder over a wide range of speeds dependent on the particular process being carried out. In a sense, each layer operation is a 'batch operation', capable of *in situ* verification rather than attempting to process long lengths continually. For some processes the cylinder may be rotated quite slowly, for example during a laser machining process to 'scribe' a helical coil, whilst for others it may be rotated quite fast, for example during thermal evaporation of YBCO when oxygenation may be taking place at the 'rear' surface of the rotating cylinder. Of course, a layer interconnection scheme (series or parallel) will have to be implemented.

3. Feasibility study

Although epitaxial YBCO multi-layers have been routinely deposited on single-crystal substrates, on the scale of tens of nanometres, to produce research and device structures for electronic applications, little or no work has been reported on multi-layer YBCO growth on biaxially textured metallic substrates. This is largely because the drive for such research has not arisen until now. Furthermore, for the present requirements the layer thickness typically would be an order of magnitude, or more, greater. Preliminary results have been obtained for the deposition of YBCO/$SrTiO_3$(STO) multilayers (>100 nm) on curved, buffered, textured Ni substrates by PLD, as reported below.

A conventional flat heater plate was replaced by a rotatable cylindrical substrate heater, 30 mm in diameter, surrounded by an independently mounted radiation shield, with an aperture to allow access for the laser plume as shown in figure 2. The rotating cylindrical heated former, with its coaxial geometry and fixed radiation shield, provides superior temperature control over that achievable for deposition onto a moving flat tape. Deposition conditions were the same as for optimized flat tapes [15]. The standard CeO_2/YSZ/CeO_2 (C/Y/C) buffer layer architecture was deposited onto biaxial Ni initially under reducing conditions at 700 °C and laser fluence of 1.5 J cm^{-2}. The target–substrate distance was 6 cm, and for the YBCO/STO layers the deposition temperature was 780 °C, O_2 pressure of 0.6 mbar, cooling down at 10 °C min^{-1} in 700 mbar oxygen after ablation. The tapes were assessed by XRD, SEM, TEM and ac susceptibility.

A single YBCO layer (∼200 nm) on standard C/Y/C buffers was initially deposited without any rotation onto a short length of textured Ni secured with silver paint onto the cylindrical heater. XRD analysis revealed only (001) peaks from the CeO_2, YSZ and YBCO with no evidence of NiO (figure 3). A T_c onset of ∼86 K was measured

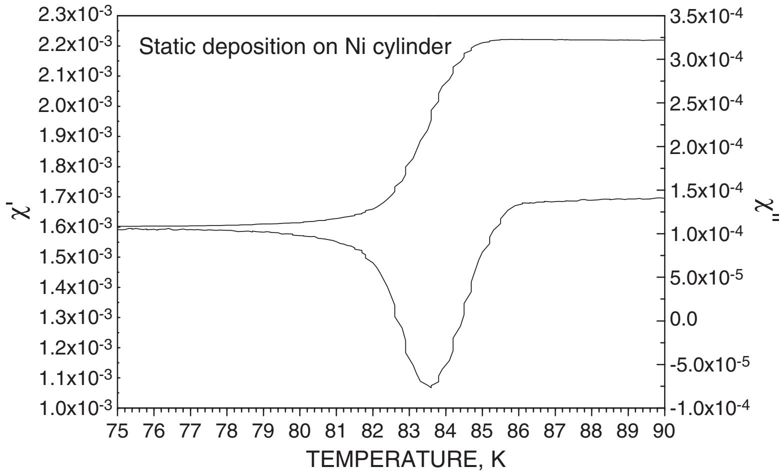

Figure 4. AC susceptibility measurement on a single YBCO layer deposited statically on a curved Ni tape.

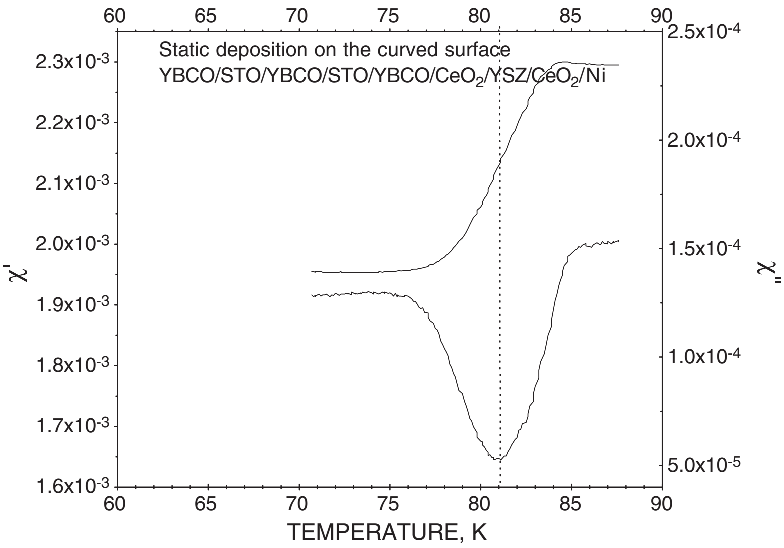

Figure 5. AC susceptibility measurement on a triple YBCO layer deposited statically on a curved Ni tape.

by ac susceptibility (figure 4). This result demonstrates the feasibility of textured growth on curved surfaces. Double and triple YBCO layers were subsequently grown with no substrate rotation on buffered Ni, with STO (~200 nm) as the intermediate layers. The T_c onset in double and triple superconducting structures was again ~86 K, but with a slightly broader transition width of 3–5 K (figure 5). XRD patterns again showed excellent *c*-axis texture.

The growth of a partially circumferential single YBCO layer on standard C/Y/C buffered Ni was then achieved by rotation of the heater assembly by approximately 180° during deposition. The rotation speed was 0.25 rpm and 38 oscillations were required to grow a 200 nm thick YBCO layer. After deposition of this first superconducting layer, rotation of the heater was stopped and the STO and second YBCO layer were deposited statically only over a ~1 cm^2 area. This enabled the properties of the first and second superconducting layers to be independently assessed. XRD showed good out-of-plane texture for both YBCO layers and T_c onset was high for both layers (~86 K). The transition width for the first layer was sharp (~2 K), but for reasons that are not clear the transition width for the second layer was much broader. The possibility of degradation associated with the increased deposition times, necessary to cover the larger area of tape by rotation, will require verification. Transport J_c measurements have not yet been attempted until further optimization of the multi-layer process has been achieved.

The defect microstructure of the tapes and the nature of the layer interfaces have been studied by cross-sectional TEM. Figure 6 shows a low magnification TEM image of a cross-section of the triple YBCO layer grown on a static curved surface. The first YBCO layer was thicker (325 nm) than the subsequent layers (175 nm) even though the number of pulses and other growth conditions were the same. The buffer layers were thinner (15, 150, 10 nm) than is usual for deposition on a flat substrate (40, 200, 40 nm) under the same conditions; the reason for this is not clear. Selected area diffraction patterns taken from the interfacial regions confirmed the copying of the biaxial texture from the Ni through to the first YBCO layer, as shown in figure 7. The (100) Ni pattern corresponds to the (110) pattern from both the CeO_2 and YSZ layers representing the well known 45° rotation, but the (100)/(010) orientation

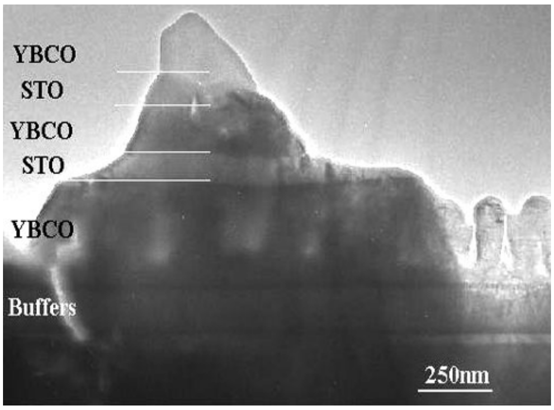

Figure 6. TEM image of YBCO triple layer.

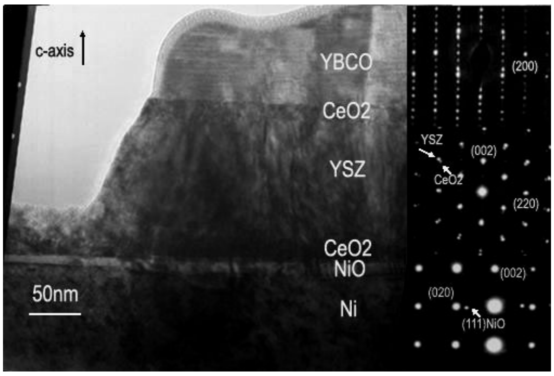

Figure 7. TEM image of buffer layer/YBCO structure together with corresponding diffraction patterns confirming transmission of the biaxial texture through the layers.

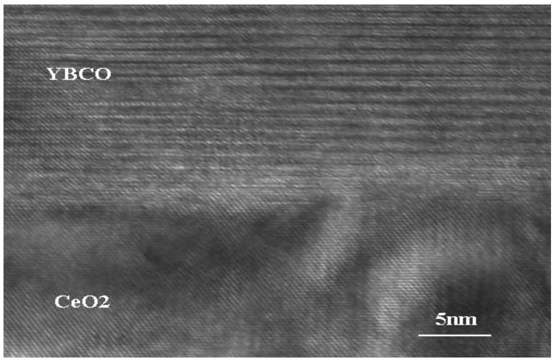

Figure 8. High resolution TEM image of YBCO/CeO_2 interface.

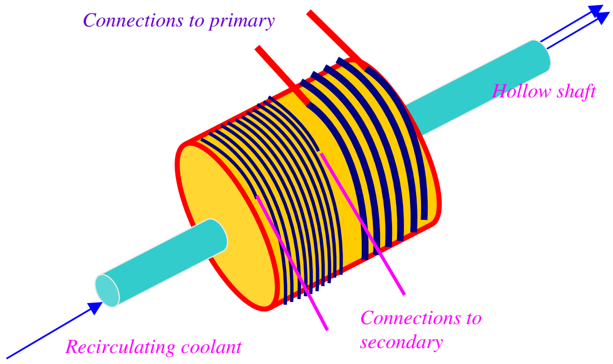

Figure 9. Proposed single-layer test structure—for a step-up transformer in this case. Similar structures could be used to demonstrate FCL devices (resistive and inductive), micro-SMES modules and a linear motor module.

is restored in the subsequent YBCO layer. Similar patterns were obtained from the subsequent YBCO layers, confirming multi-layer epitaxy. The NiO layer revealed a (111) orientation with respect to the Ni(010) substrate. This non-epitaxial relationship is consistent with the NiO layer being formed after the growth of the epitaxial CeO_2 seed layer, most probably during the growth of the YBCO layers [16]. The thickness of the NiO layer was considerably greater on the curved surface than on a flat surface, as shown in figure 7, probably due to the increased time at elevated temperature associated with the triple-YBCO-layer deposition.

Some evidence for small *a*-axis regions, stacking faults and interfacial dislocations was observed, but the majority of the interfaces were of high quality. Figure 8 shows an HREM image of the CeO_2/YBCO interface. There was no obvious evidence of any reaction between the YBCO and CeO_2 to form the recently observed $BaCeO_3$ [14], nor the presence of any disordered perovskite layer within the YBCO. The interface was atomically sharp and the surface of the CeO_2 was flat, ideal for growing highly *c*-axis oriented YBCO.

Although some optimization is required the principle of growth of epitaxial superconducting multi-layers on curved Ni surfaces has been established by these results.

4. Implications for systems design

The ability to define the geometry of conductor tracks on the surface of the cylinder, rather than being constrained by the tape geometry, gives the design engineer increased degrees of freedom. Two more important advantages of the present cylindrical processing approach from a systems viewpoint are that it allows higher engineering current densities and reduced ac losses. This is because there is no repetitive wasted substrate to reduce the engineering J_c and add to the losses, unlike conventional tape winding. Higher engineering current densities should result in electrical machines of reduced size and weight. Also, as a result of the increased structural integrity and the integrated manufacturing approach, refrigeration may even take the form of liquid nitrogen or gaseous helium circulated through pathways within the cylinder and its shaft, i.e. integrated refrigeration.

Quite simple single-layer demonstrators could be fabricated using the new approach, and one of these is shown in figure 9. Using essentially the same processing technology, a number of different functions can be realized from the same structure. It is interesting to note that the fabrication of similar structures using the conventional coated conductor tape approach would involve many reel-to-reel processing steps and final coil winding, none of these steps being required in the new approach. Of course it is recognized that a multilayer structure will require a great deal more materials research, particularly for the joining technology between layers. Such a joining technology could incorporate weak links in the form of FCL devices already positioned within the cylindrical substrate, or located at the ends of the cylinder. It is possible to envisage a new generation of electrical machines based on cylindrical modules of a standard size, say 15 cm long and 8 cm in diameter. These basic 'building blocks' can be arranged to form, for example, a multi-module SMES unit, an array of magnets for one-sided MRI, a multi-module coaxial transformer or an array of modules for a motor or generator. The possibilities are many and intriguing.

The standardized module approach has many economic benefits as the rapid growth of the semiconductor industry has shown. Today's chip processor, containing tens of millions of transistor building blocks, seems light years away from the original point contact transistor, demonstrated in 1948, but a direct route can be traced back. There were many radical shifts in thinking required throughout this period, and that is what we are advocating here—a careful re-examination of the goals for HTSs.

5. Conclusions

A new integrated manufacturing approach to coated conductor devices has been described which could result in standardized coated conductor modules for power systems designers. This could dramatically shorten the time to market for HTS electrical machines. The general approach is more closely allied to the semiconductor industry than to the industry which has built up around low temperature superconductors, and represents a radical shift in direction for commercialization of HTS components.

The epitaxial deposition of YBCO/STO multi-layers on a textured curved Ni tape has been reported, which demonstrates the proof of principle of multi-layer coil fabrication on this and alternative textured curved substrates.

References

[1] Goyal A *et al* 1996 *Appl. Phys. Lett.* **69** 1795–7

[2] Norton D P *et al* 1996 *Science* **274** 755–61

[3] Iijima Y, Tanabe N, Kohno O and Ikeno Y 1992 *Appl. Phys. Lett.* **60** 769–71

[4] Wu X D *et al* 1995 *Appl. Phys. Lett.* **67** 2397–9

[5] Freyhardt H, Hoffmann J, Weismann J, Dzick J, Heinemann K, Isaaev A, Garcia-Moreno F, Sievers S and Usoskin A 1997 *IEEE Trans. Appl. Supercond.* **7** 1426–31

[6] Hasegawa K, Fujino K, Mukai H, Konishi M, Hayashi K, Sato K, Honjo S, Sato Y, Ishii H and Iwata Y 1996 *Appl. Supercond.* **4** 487–93

[7] Tixador P, Donnier-Valentin G, Trollier T, Michellier L, Maher E and Usoskin A 2003 *EUCAS 2003*; *Supercond. Sci. Technol.* submitted

[8] Maher E F 2003 *International Patent Application* PCT/GB02/03898 (published as WO 03/019589)

[9] Nemetschek R, Prusseit W, Holzapfel B, Eickemeyer J, DeBoer B, Miller U and Maher E 2002 *Physica* C **372–376** 880–2

[10] Denul J, de Winter G and Gryse R D 2001 *IEEE Trans. Appl. Supercond.* **11** 2909

[11] Yamada Y, Suga T, Kurosaki H, Kim S B, Maeda T, Tamada Y, Hirabyashi I, Yamazaki M, Yoshino H and Watanabe T 2002 *Physica* C **372–376** 828

[12] Ignatiev A, Zhong Q, Chou P C, Zhang X, Liu J R and Chu W K 1997 *Appl. Phys. Lett.* **70** 1474

[13] Shields T C, Abell J S, Button T W, Chakalov R A, Chakalova R I, Cai C, Haessler W, Eickemeyer J and de Boer B 2002 *Physica* C **372–376** 747

[14] Chakalova R I, Cai C, Woodcock T, Button T W, Abell J S and Maher E F 2002 *Physica* C **372–376** 846–50

[15] Kakihana M 1996 *J. Sol–Gel Sci. Technol.* **6** 7

[16] Leonard K J, Goyal A, Kroeger D M, Jones J W, Kang S, Rutter N, Paranthaman M and Lee D F 2003 *J. Mater. Res.* **18** 1109–22